Annual Work Programme 2008

Preface

This document was prepared by the AENEAS association of R&D actors in the field of ENIAC and further edited under the responsibility of the interim Executive Director on behalf of the ENIAC Joint Undertaking. It is to be read in conjunction with the Strategic Research Agenda of the European Technology Platform ENIAC; the draft edition of the ENIAC Multi-Annual Strategic Plan issued in March 2008, and Council Regulation 72/2008 of December 20, 2007, describing the rules and procedures of the ENIAC Joint Undertaking.

This Work Programme has been developed on the basis of consultations with the research and industrial community which included the participation of SMEs, and with the help of a questionnaire, first to establish the ENIAC Strategic Research Agenda (SRA), then the Joint Undertaking Multi-Annual Strategic Plan and the Annual Work Programme 2008.

Content

1 Introduction

1.1 The context

Nanoelectronics is the essential hardware enabler for the innovation of electronic products and services in key growth markets for the European industry. In 2004 a High Level Group of key representatives published its 'Vision 2020' for nanoelectronics and launched ENIAC, the European Technology Platform for Nanoelectronics, with the overall aim to guarantee Europe the earliest possible access to leading-edge integrated components, miniaturized electronic (sub)systems and design skills for application in high-technology products and services, thereby reinforcing Europe's existing industrial strengths and ensuring that core intellectual property is generated and benefited from in the region. –As a result of the work of the Technology Platform, the ENIAC Strategic Research Agenda (SRA) was established through the voluntary and concerted efforts of experts from industry, academia, and public authorities across Europe. This SRA is revised regularly. Its 2nd revision was published on November 28, 2007. The ENIAC SRA is the common envelope guiding the definition and execution of R&D in nanoelectronics in Europe for all players (industry, academia, and public authorities) and all mechanisms for public-private partnership (national, transnational, and EC). Top executives of leading European companies and research organizations have signaled their full commitment to reaching the ambitious goals set out by the SRA.

Anticipating a more coordinated and efficient implementation of the R&D activities highlighted in the ENIAC SRA, a group of key stakeholders cooperating within the ENIAC Technology Platform established the AENEAS association to foster a more focused participation of all industrial and academic stakeholders actively engaged in the definition and execution of nanoelectronics R&D in Europe.

In order to execute part of the cooperative research and development activities required to fulfill the SRA, a dedicated entity was established as the concrete implementation of a public-private partnership between industry, grouped in the AENEAS association, several Member States and the European Commission. That entity, called the ENIAC Joint Undertaking (JU), was set up by Council Regulation 72/2008 of December 20, 2007, aiming at combining the public and private efforts needed for resolving the downstream-oriented research priorities in the ENIAC SRA.

The statutes of the JU are annexed to the Council Regulation 72/2008[1] and the rules and procedures of the AENEAS association are described in the Articles of Association[2].

The bodies of the ENIAC JU consist of a Governing Board (GB), a Public Authorities Board (PAB) and an Industry and Research Committee (IRC), each with their own tasks and responsibilities.

The Council Regulation states that the Joint Undertaking will have its own Research Agenda (RA). The Research Agenda of the JU closely follows the recommendations of the Strategic Research Agenda of the ENIAC Technology Platform. It addresses the downstream activities related to equipment, materials and processes, the manufacturing and design of nanoelectronics components and miniaturized (sub)systems, and their use in various application fields.

The JU RA is a subset of the ENIAC SRA since other European and national programmes – including Eureka - also contribute to the goals of the ENIAC SRA, as well as individual industrial and academic research activities. Therefore, no additional document was generated.. In particular, the ENIAC RA focuses on research that can deliver prototype or demonstrator solutions with high cross-domain applicability to address specific and important societal needs. The more upstream activities and some very specific activities complementary to the JU cooperative research activities are planned to be covered under the regular Framework Programme 7 type of activities or by research in institutes, universities and companies funded by the individual Member States.

[1] OJ L 30 4.2.2008, p. 21

[2] http://www.eniac.eu/web/downloads/aeneas/AENEAS%20AoA%20English.pdf

1.2 The JU research strategy

In the statutes of the ENIAC JU, a Multi-Annual Strategic Plan (MASP) is foreseen, which defines the strategy that the JU will follow to ensure that the RA can be executed under the most favorable conditions: how the RA can be supported, how it will be financed, and how it will be managed. The AENEAS association is chartered by the IRC to draft this MASP[3] that outlines the JU strategy and plan as it evolves over time as a function of research priorities and stakeholder commitments.

The selection of topics within the MASP is primarily along the axis of long-term societal needs and lead markets. The six societal segments identified in the ENIAC SRA are Health & Wellness, Transport & Mobility, Security & Safety, Energy & Environment, Communication, and Infotainment, leading to segmentation in six application-specific Sub-Programmes in the MASP (respectively SP1 to SP6). Many of the challenges listed in the ENIAC SRA technology domains can be mapped on the applications in these lead markets, notably topics from More Moore, More than Moore, and Heterogeneous Integration. It should be recognized that commonalities continue to exist in many basic technologies underlying the various application-specific Sub-Programmes. Also the priorities within these technologies can be the same, the difference being the timing or the level of maturity needed. However, in the technology domains Design Methods and Tools, and Equipment and Materials, cross-domain and cross-application aspects are dominant. Challenges in these domains can be better handled as generic enablers, serving all ENIAC societal needs and lead markets. Therefore, the application specific Sub-Programmes SP1 to SP6 in the MASP to cover the RA are complemented with two Sub-Programmes SP7 and SP8 that are technology-specific, bringing the total to eight. The mixture of technology- and application-driven Sub-Programmes, seeking maximum synergy between the various application Sub-Programmes while at the same time recognizing their individual socio-economic value and their capability to drive wider technological progress, will guarantee an efficient set-up of the entire programme.

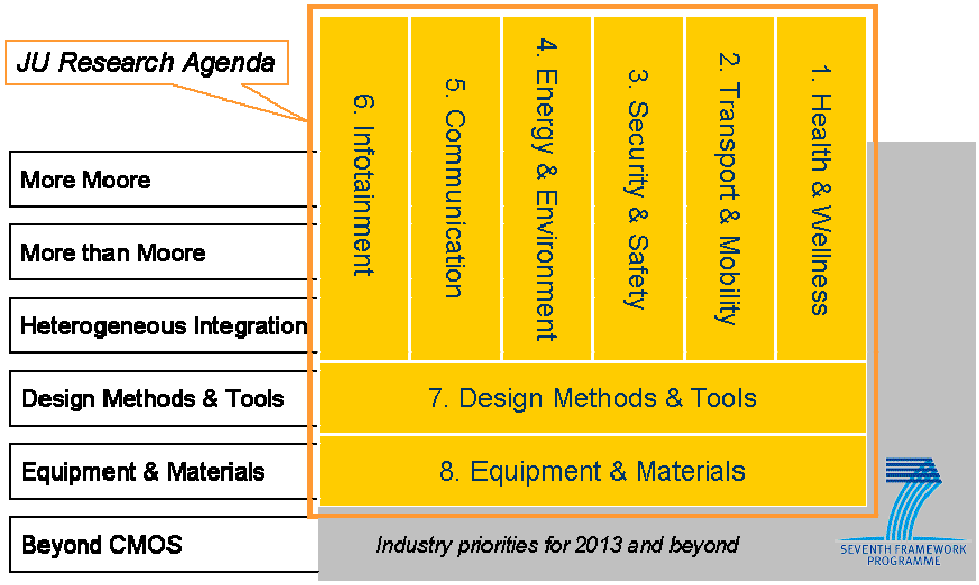

Figure 1 – Mapping the JU RA on the SRA technology domains

Not covered in the MASP are the upstream oriented R&D priorities identified by the ENIAC SRA for the period beyond 2013 in the domain More Moore, More than Moore and Heterogeneous Integration and most of the content listed for the technology domain Beyond

[3] Document ENIAC-MASP-1

CMOS. These priorities are recommended for inclusion in the coming calls in the regular FP7. Also specific supporting activities related to equipment assessment, standards, international cooperation, etc… are to be covered in FP7. Furthermore some activities related to the research on the most advanced process technologies which are better executed in a wider international context are also not directly covered. Further synergy exists with the more application-oriented activities in CATRENE (EUREKA cluster project 4140) and with the embedded systems covered by the ARTEMIS JU.

It is planned to update the MASP and have it agreed by the GB in the same frequency as that of the ENIAC SRA that is every two years. A new revision is also forecasted by end of 2008.

1.3 The priorities for 2008

In connection with the MASP, the IRC also proposes the Annual Work Programmes (AWP) of the JU, which defines on a yearly basis the specific objectives for R&D to be achieved through Calls for Proposals. The AWP and related calls are adopted by the PAB which also commits the needed financial resources for each call.

The present document is the Annual Work Programme for 2008. It defines the content and scope of the single Call for Proposals focusing on downstream-oriented research to be launched in 2008. The text of the Call for Proposals will further detail the available budget and the eligibility criteria, taking into account the requirements of both the European Commission and ENIAC member States.

The ultimate choice of topics to be included is done in close consultation with all public and private stakeholders. Leading criteria for selection are the targeted budget for this Call, the industrial urgency, synergy with other JUs (notably ARTEMIS, Innovative Medicines, and Clean Sky), synergy with adjacent European Technology Platforms (notably EPoSS and Photonics21), readiness of the industry to engage into major initiatives, and alignment with national and EC policies.

The selection of a limited set of Sub-Programmes from the Multi-Annual Strategic Plan leads first to keep the two transversal Sub-Programmes open, since they are essential to nurture the technological competencies in design and manufacturing which help ensure the completeness of the value chain in Europe. Within these Sub-Programmes, indications are given regarding some R&D orientations that seem currently important. This allows a further prioritizing within the Sub-Programmes.

Among the application Sub-Programmes, a selection was achieved and clearly announced to stakeholders since December 2007. A guiding principle in the sub-programme focusing was to some extent the commonalities that exist between the semiconductor technologies that power the corresponding application field. For instance power electronics can contribute both to SP2 Transport & Mobility and to SP4 Energy & Environment. Furthermore these application fields drive technologies and competencies which have a high potential for wider applicability and spill-over results in different sectors. Within these Sub-Programmes indications are given regarding major short and mid term R&D needs calling for industrially driven projects of high economic or socio-economic relevance.

This focused selection is large enough to allow a number of good proposals and also to allow other Sub-Programmes to be addressed within the call of 2009. A more focused approach would have led to a wait time of 2 years for entire Sub-Programmes which probably would have excluded significant actors for a too long duration.

This prioritization amongst Sub-Programmes and within Sub-Programmes will be a continuous process. For the upcoming years the process is planned to be the following. In 2009 there will be a call concerning SP1 Health & Wellness, SP5 Communication, SP6 Infotainment, SP7 Design methods and tools, and SP8 Equipment & Materials. At the same time, taking the expected increase in budget into account there will be additional provisions to cover:

- Satellite projects to complement the larger ones already started,
- Re-opening of a selection of specific topics from other SPs where it is felt that the coverage is not broad enough.

The present document summarizes the priorities for the 2008 ENIAC AWP as identified by the IRC and adopted by the PAB of the JU on the basis of the guidance provided by the current MASP and field interviews within representatives of the AENEAS members and other stakeholders in the nanoelectronics R&D ecosystem. It covers 3 application oriented Sub-Programmes and the 2 technology-driven Sub-Programmes. Within each of these, a set of target activities gives further focus and indications regarding major short and mid term R&D needs. Each of the topics listed is a relevant research priority item contributing to resolving the market- and society-driven technology challenges for the corresponding ENIAC sub-programme, calling for industrially-driven projects of high economic or socio-economic relevance. A section on synergy with other priorities underlines the importance to address activities with a wide application or cross-cutting potential. Each proposal should address at least one target activity in one sub-programme and clearly identify which ones have been addressed. The expected industrial or socio-economic impact is highlighted. Proposals should demonstrate how they will generate such direct or indirect impact. Indications towards a targeted approach are given as guidance for potential proposers.

It should be kept in mind that wording, size and duration of the items in the list are illustrations for the priorities, not specifications for the expected projects.

In line with the objectives of a Joint Technology Initiative, offering the potential for larger Europe-wide initiatives, with more flexibility, increased efficiency, no restriction in duration or size, it is expected that a vast majority of large, integrated projects are launched in order to have a significant industrial impact and to demonstrate sufficient critical mass The consortium size or amount of resources is naturally also dependent and should be guided by the topic and needs of the proposed project. Some Sub-Programmes or target activities may also be covered by a mixture of projects of different sizes.

Within each integrated project, a realistic representation should be found for the underlying nanoelectronics R&D ecosystem in Europe, including large corporations, SMEs, institutes, and universities. The mechanisms to accommodate smaller partners, SMEs, institutes or universities in larger integrated projects can vary from direct participation in the project to subcontracting with one of the direct project partners, or via a set of linked smaller projects. Such linked activities or projects could also be accommodated through other calls for proposals in the year following the start of the large projects.

The manpower amount indicated, a total of 2000 person/years, can obviously not be reached in terms of funded projects in each and every sub-programme for the first year, and the repartition will be adjusted depending on the quality of project proposals. It is just a rough indication of the estimated size it could have if the subtopics outlined for this first year would all be covered in a specific sub-programme. It does not take into account potential synergy between the different Sub-Programmes or target initiatives. The proposals should anyhow largely exceed these figures. This approach might evolve over time depending on the feedbacks.

2 R&D Sub-Programmes – priorities 2008

2.1 SP2 - Nanoelectronics for Transport & Mobility

Introduction

The most urgent priorities in the field of Automotive Electronics are the reduction of fuel consumption, driven by increasing costs of oil and environmental concerns, and the need to increase safety on the roads, in spite of ever increasing traffic density.

Target activities

Both short term and long term research activities in the field of Nanoelectronics are required to enable the roadmaps defined by the Technology Platform for Automotive ERTRAC and in line with the SRA of the eRTD working Group of the eSafety Forum.

Industrially driven projects for Nanoelectronics Research for Transport and Mobility will address the areas of:

- **Components and miniaturized (sub)systems for Assisted driving** to increase car safety and reduce collision risk. To comply with the users' requirements there is the need to develop a variety of sensors and increase road awareness: high dynamic range optical system, car-radar systems, infrared sensors or light amplification for foggy or night vision. Increasing complexity and reliability of the data processing system will allow moving from simple warning of potential risks, to the automatic implementation of corrective measures. Distributed sensor networks will be required and System-in-Package technology will be increasingly used to reduce the costs of sensors.
- **Technology, components and miniaturized (sub)systems for advanced engine control systems and exhaust and combustion control.** Reduction of pollution levels and consumptions requires, in the short term, the development of advanced engine control systems for combustion engines, to reach the target of a 30% reduction in average CO2 emissions for the new vehicle fleet in 2020. The requirement will be for the development of more powerful control units with Non Volatile Memory, to allow for engine regime optimization under different traffic and environment conditions. Smart power will be required for the control of mechatronics, and chemical sensors would be needed for exhaust and combustion control. High temperature reliability and zero failure rate will be required for all components.
- **Power and high voltage electronics and smart miniaturized systems for hybrid and electrical cars.** Electrical cars will be a longer term solution. They require the development of power and high voltage electronics for power management and engine control and energy recovery systems. Smart power control logic is required to manage the energy flow between batteries and super-capacitors, and between the storage systems and the engines. Mechanical sensors are needed to implement a full control of the car system, especially in view of the integration of the engines with the wheels.
- **Development of fail safe and fault tolerant electronic systems** is a cross functional priority, which applies to all existing car electronics, and to all technologies to be developed in the above mentioned projects. To reach this target new methods and technologies for improved reliability and increased lifetime are needed. The requirement is for the analysis of failure mechanisms of different technologies under harsh conditions, the development of accelerated life tests and screening procedures and the implementation of fail safe design methodologies.

Synergy with other priorities

Possible synergy areas with other priorities are (not exhaustive):

- Basic power and power management technology will also find use in the Sub-Programme 4: “Energy and Environment, for the control of Industrial Electronics”.
- Optical sensors will be a basic technology usable also in the Sub-Programme 3: “Nanoelectronics for Security and Safety”, even if the requirements for reliability and dynamic range will be tougher for Automotive applications.
- Safe design methodology, and Design for Reliability can profit from the results of the priority “Device, circuit, and system variability and reliability” in the Sub-Programme 7: “Design Methods and Tools for Nanoelectronics”
- System-in-Package technology will profit from the results of the priority “Assembling technology for system-in-package” in the Sub-Programme 8 “Equipment and Materials for Nanoelectronics”, even if it will require a dedicated effort for temperature control and heat management

Expected impact

Expected industrial impact relates directly to increased competitiveness of the semiconductor and the automotive industry in key lead markets. Other closely related industries such as avionics, industrial electronics or industrial equipments operating in harsh environments or requiring high reliability considerations will also benefit.

Direct social impact is also expected on mobility policy, safety and on sustainability (environmental) policies.

Targeted Approach

Large scale projects are targeted that could start within the first year in these areas or crossing these areas, developing basic technology until demonstration in a final system, involving the cooperation of user companies (automotive equipment and car manufacturers), semiconductor companies, design houses, assembling and packaging companies and relevant research institutes and universities. These main projects should show both vertical integration with the final user and with equipment, materials and design providers and horizontal cooperation to build a solid technology base for Europe and establish standards.

The backbone of these projects is expected to be formed by large companies, which will stimulate and organize the participation of SMEs and be supported by Research Centers and Universities. The large scale projects will be complemented by smaller focused projects, also through the use of side calls at a later stage, with a large potential for SME and institute contribution.

Synergy should be established with other Subprograms, for the development of a common, cross-functional technology base

Indicative resources

500 PY for all SP2 target activities, representing 25% of the overall Work Programme.

Targeted start date of the projects: end 2008.

2.2 SP3 - Nanoelectronics for Security & Safety

Introduction

Security and safety is one of the major requirements for society in virtually every aspect of our lives reflecting itself in public demand for personal emergency and home security systems, and for government led protection from crime and terrorism. Moreover automatic systems are penetrating in many life sensitive applications such as in transport or health related systems putting very high requirements on the related safety aspect.

Target activities

Short and long term activities to enable new safety and security systems that need to be reliable, secure, safe, fault tolerant, easy to use and capable of safeguarding the privacy of end users.

Industrially driven projects for Nanoelectronics Research for Security and Safety will address the areas of:

- **Trusted devices and smart secure portable objects**, will address systems aspects like multi-level security architectures, secure computing techniques*;* separation of concerns and specific middleware, and new hardware technologies like new memory architectures, memory management units, digital rights management units, processors and cryptographic, resistance to side-channel attacks, anti-tampering coating and packaging on–chip batteries. Segregated wireline and wireless I/Os and internal firewalls. Encrypting, passwords and access control management.
- **All-in-one imaging sensors**, including emission and active imaging, detection, processing in focal point, pupil post processing and tracking treatments. Cameras and sensors related to radar, infrared, acoustic or optical systems. Nano-electromechanical devices applied in sensors.

Synergy with other priorities

Possible synergy areas with other priorities are:

- Basic new memory architectures, processors and basic technology for encrypting, access control will find their use in all other Sub-Programme priorities and also use in the Sub-Programme 2 "Transport and Mobility" and in Sub-Programme 5 " Communication" and 6 "Infotainment" and in Sub-Programme 4 “Energy and Environment”.
- Optical sensors will be a basic technology usable also in the Subprojects 2: “Transport and Mobility”, even if the requirements for reliability and dynamic range will be tougher for automotive applications.
- Safe design methodology, and Design for Reliability can profit from the results of the Sub-Programme 7: “Design Methods and Tools for Nanoelectronics”; programming methods and middleware have a direct synergy with activities going on in the relevant Sub-Programme in ARTEMIS.

Expected impact

Direct industrial impact is expected in personal emergency and home security systems, in increased safety and security as a generic enabler for many other applications and related services in transport, health, banking, identification, telecommunication, safety critical systems and for government led protection from crime and terrorism.

Targeted Approach

Large scale initiatives are targeted that could start within the first year in these areas or crossing these areas, developing basic technology as a common building block ("trusted devices"). From this common element, various application segments can be addressed.

Such projects should include basic technology developments until a demonstration in a final application, involving the cooperation of user companies, semiconductor companies, design houses, assembling and packaging companies and relevant research institutes and universities. The main projects should show vertical integration as well as the potential to spread developments over a wider application domain.

It is expected that the project(s) will be formed by a combination of large companies and SMEs and be supported by Research Centers and Universities. The initiative could further include or be complemented by smaller focused projects, with potential for a large SME and a large institute contribution.

Synergy should be established with other Subprograms, for the development of a common, cross-functional technology base

Indicative resources

200 PY for all SP3 target activities, representing 10% of the overall Work Programme.

Targeted start date of the projects: end 2008.

2.3 SP4 - Nanoelectronics for Energy & Environment

Introduction

Efficient use of energy and waste reduction are the political, social and technical challenge of the next decade. Focusing on micro-/ nanoelectronics approaches, efficient power supply and intelligent energy control in new products can reduce electrical energy consumption in Europe by 20% to 30 % until 2020 by simultaneous increase of safety, functionality and convenience. This will reduce CO_2 emission in the same order of magnitude in order to achieve the Kyoto protocol targets and will limit the energy cost increase.

Target activities

Both short and mid term activities to provide innovative technologies as the basis for new energy efficient products and intelligent power management to enable increased competence in these emerging lead markets in line with the 'sustainability' objective[4].

Industrially driven projects for Nanoelectronics Research for Energy and Environment will address the areas of:

- **Intelligent drive control.** Technology, components and miniaturized (sub)systems addressing the challenges at system and device level for highly efficient controlled engines and electrical actuation in industrial applications. The need for R&D includes new systems architectures and circuit designs; new components and power electronic technologies; innovative module, interconnect and assembly technologies.

- Efficient **power supplies** and **power management solutions,** combining the measures for voltage conversion and stand-by. The need for R&D includes new systems architectures and innovative circuit design concepts and specific driver ICs and power components for lighting and industrial equipments.

Synergy with other priorities

Synergy could be established with other Subprograms, for the development of a common, cross-functional technology base. Possible synergy areas with other priorities are:

- Power management technology and intelligent drive control will also be used in the Sub-Programme 2: “Nanoelectronics for transport and mobility”.
- Synergies with design platform activities in the design of efficient power supplies, high reliability solutions, design for operation under harsh conditions.
- Synergies with equipment and materials in relation to high power electronics. Completely new or improved semiconductor technologies, using leading edge technology knowledge for low power consumption and extended lifetime (e.g. high frequent and low-loss switching, digital power conversion). New semiconductor materials like SiC or GaN, thin substrates and interconnect materials to improve performance and reduce cost. In-package integration of power devices and control logic.

Expected impact

Direct impact is expected on the automotive industry, on automation and on industrial equipment and home appliances. Direct contribution should go to various environmental and sustainability policies at national and European level.

[4] Current Sustainable Development Strategy (2006): European Council *DOC 10917/06*

Targeted approach

Large scale projects are targeted that could start within the first year in these areas, developing basic technology until demonstration in a real environment, involving the cooperation of user companies. These main projects should show both vertical integration with the final user and with equipment, materials and design providers and horizontal cooperation to build a solid technology base for Europe and establish standards.

It is expected that the back-bone of the projects will be formed by large companies, which will stimulate and organize the participation of SMEs and be supported by Research Centers and Universities. The large scale projects could be complemented by a cluster of smaller focused projects, also through calls in a second phase, with larger SME contribution. Synergy must be established with other Sub-Programmes for the development of a common cross functional technology base.

Indicative resources

400 PY for all SP4 target activities, representing 20% of the overall Work Programme.

Target start date of projects: end 2008 – begin 2009.

2.4 SP7 - Design Methods and Tools for Nanoelectronics

Introduction

Design Methods and Tools for Nanoelectronics are needed to bridge the gap between technology and design capability created by the growing design gap (due to technology improving density by a factor 2 every 18 months and design tools improving productivity only by a factor 2 every 5 years) and to address the increasing complexity of devices in terms of density and integration of, different technologies and functions in the same system. Moving to nano-scale technologies not only results in all the design steps, from specification down to fabrication, becoming strongly interdependent. It also results in them being intimately linked to yield, variability and reliability

Target activities

Short and mid term activities are required to enable the efficient design of advanced components, Systems on chip, Systems in a Package and compact miniaturized electronic (sub)systems.

Industrially driven projects for Design Methods and Tools for Nanoelectronics will address the areas of:

- **Device, circuit, and system variability and reliability.** Design methodology will need to cover and connect all aspects of physical design, at different levels. Detailed physics-based models in TCAD tools need to include the impact of device variability on reliability. Mixed mode device/circuit TCAD tools are demanded to assess the impact of device degradation on the functionality of fundamental circuit building blocks. Accurate characterization methodologies of devices, circuits and sub-systems need to support physical models of variability impact on performance, timing, power and yield. Fast and reliable extraction procedures of parameter fluctuations and proper methodologies are necessary to bridge experimental results on devices, measured in parallel and physical models of rare events at the highest level. New paradigms in system design have to be developed, related to variability that would enable to realize reliable, complex products using unreliable and variable devices. Research is needed on fault-tolerant architectures with redundancy and self-repairing features to provide methods of coping with statistical variability and reliability limitations.

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- **Hardware/software model driven hi-level synthesis/flow/reuse/design.** Design platforms have to be developed that would allow for system HW/SW partitioning and a complete design flow enabling continuity from application SW down to silicon realization allowing mastering the ever growing complexity of nanoelectronics systems. Methods for the flexible IP blocks reuse by HW dependent SW, Design for Manufacturing and Design for Testability are necessary for all technology domains.

Synergy with other priorities

- Specific TCAD, modeling, simulation and design activities will be embedded in most application projects. However larger initiatives are needed to develop tools and methodologies of common interest, applicable to all device and system environments, including analog/mixed signal, digital logic, and embedded as well as stand-alone memories. These tools and methodologies will further be used and demonstrated in the application specific Sub Programs.
- Synergy is further expected with the design platform activities in ARTEMIS.
- Research on fault-tolerant architectures with redundancy and self-repairing features is also highly relevant to Sub-Programme 2: “Transport and mobility”.

Expected impact

These short-term design activities are the prerequisite for the longer-term vision, to provide industry with design methodologies and tools which span from semiconductor technology including statistical variability, through devices and circuits to whole systems integration in package, and to make available all technology-related data to enable Design for Manufacturing, Design for Testability, Design for Reliability, and finally Design for Yield. Creating a strong link between technology and design is the long-term vision that will require an increase in efficiency of design tools to cope with the largely increased complexity of the devices in terms of density and multi-functionality.

The results will have a direct industrial impact for design houses, design units in Integrated Device Manufacturer (IDM's), semiconductor companies and CAD tool vendors. They will impact the design time, quality and efficiency of the design process and allow the first time right design of complex components, subsystems and products in all application fields.

Targeted approach

Large scale projects as well as smaller focused projects - if the suggested R&D content is significantly supportive to achieve the goals are targeted that could start the first year in the described areas, developing methods, models and tools and incorporation in the design platforms, involving the cooperation of user companies (IDMs, fabless), design centers and CAD tool developers, universities and institutes. The main projects should show the integration of the resulting technologies, to build a solid electronics design base for Europe and establish standards.

It is expected that the back-bone of the projects will be formed by a combination of large companies and SMEs active in the EDA and design area and be supported by Research Centers and Universities. The projects could offer space to the growth of specialized EDA start-ups, also through the aggregation of smaller focused projects for the main ones.

Synergy should be established with other Subprograms, since the design is an integral part of all electronics products.

Indicative resources

300 PY for all SP7 target activities, representing 15% of the overall Work Programme.

Projects expected to start end of 2008, begin 2009.

2.5 SP8 - Equipment & Materials for Nanoelectronics

Introduction

The activities in R&D for manufacturing, equipment and materials have to strengthen the capability for Europe to maintain and develop a profitable and consistent manufacturing base of key strategic relevance both in economic and political terms. They will need to strengthen the semiconductor companies, giving access to the most advanced manufacturing methodology and allowing equipment and material companies to play a significant role in global alliances and in developing local ecosystems. A high level of co-operation is required between the innovators, equipment manufacturers and manufacturing organisations. Special attention is also given to the replacement of toxic materials, the reduction of energy and water consumption, and, in general, to reducing the impact of the manufacturing process on the environment.

Target activities

Both short term and mid term research activities are required to enable that the European semiconductor component and (sub) systems industry remain competitive without sacrificing the sustainability of the industry.

Industrially driven projects for equipment and materials will address the areas of:

- **Advanced line operation** that match the requirements of European device makers to increase the productivity and sustainability of the most advanced CMOS and derivative technologies semiconductor fabs. This should include reducing cycle times; improving reproducibility through use of Advanced Equipment Control (AEC) and Advanced Process Control (APC) and virtual metrology; improving the equipment effectiveness, cost and efficiency, flexibility and productivity; as well as reducing environmental impact also with the introduction of analytical methods for high purity gasses & liquid chemicals.
- **Lithography process for beyond 32nm manufacturing** to support European leadership in lithography equipment and photomask technology for both optical and maskless technologies. An important element in the pre-commercial phase of these technologies is the development of standards, in order to define the interfaces that different suppliers have to use in order create a competitive and future proof platforms. Focus should be on the extension of immersion lithography with improved material and equipment, double exposure and metrology, and new resist and mask concepts.
- **R&D for assembling technology for system-in-package** to support generic process steps, like 3D related technologies: through-silicon-vias and other 3D packaging technologies, handling of ultra-thin wafers, wafer level packaging and die stacking techniques; testing and reliability for known-good-dice, die alignment and handling; innovative package and interconnection materials and technologies acting as a key competitive differentiator in the automotive and telecommunication industry, as well as in other semiconductor driven industries.

Synergy with other priorities

As equipment and materials research is focusing on moving the limits of the capabilities of the semiconductor industry at large, it enables all application domains described in the above Sub-Programmes. Development activities on Equipment and Materials are also an essential part of application-oriented projects, impacting not only functionality (e.g. for sensors) but also cost efficiency, power dissipation and reliability under harsh conditions.

Synergies are expected with several application projects:

- Assembling technology activities will be embedded in most application projects, especially in Sub-Programme 2: “Transport & mobility” and 4 “Energy & Environment”, to allow a tight integration of control logic and power handling devices, able to withstand harsh environmental conditions.

- Dedicated multichip packages are needed in Sub-Programme 3 “Security and Safety” to integrate sensors and to cope with limitations in space, interconnection complexity or power dissipation.
- Advanced substrates will be required for specific applications in Subprograms 2 and 4, such as SiC and Thick SOI for power devices, and in Sub-Programme 3, such as thin SOI for low power CMOS, as required by portable trusted devices.
- Testing equipment development is tightly related to the development of design tools and methodology in Sub-Programme 7 to have an efficient implementation of design for reliability, and design for test.

Expected Impact

Innovation in materials, equipment and advanced process and manufacturing activities are key elements for any progress in the semiconductor Industry. Projects will need to contribute to maintain the key position of European equipment suppliers in the global market and to the competitiveness and sustainability of the semiconductor fabrication in Europe.

Direct industrial impact is expected for the semiconductor equipment and materials industry. Moreover, the semiconductor equipment and materials manufacturing industry has a profound impact on developing local supplier ecosystems, thereby acting as a powerful engine for economic growth and high quality jobs.

The equipment market is also a highly competitive market, often creating spill-over effects to other high-tech industries like medical and automotive.

European semiconductor manufacturers will further benefits from “fit-for-purpose” development and manufacturing equipment to meet technology, productivity and cost requirements needed to maintain the competitiveness of a diverse and innovative range of technology niches.

Targeted approach

Equipment development projects in this field will require a tight co-operation between equipment manufacturers and manufacturing organisations, for solutions to be made available that support the quick and cost-effectively introduction of new products on the European market and increase the competitiveness of European manufacturing industry. Projects can involve different levels of the supply chain, offering opportunities for high tech SMEs. Typically equipment development projects are close collaboration between a key equipment supplier, eventually a number of component suppliers and material suppliers and eventually a leading research centre or university, and one or several strategic key lead customers that are willing to put the new development to the test. Projects in this field also offer ample space for cooperation between competing semiconductor manufacturers because of the advantage in sharing development costs of advanced equipment and materials.

There is also the potential for multiple equipment makers to work together to resolve integrated processing issues that may effect the advanced line operation and of co-operative initiatives whereby different industry sectors work together.

In manufacturing science, the industry requires also a converging network with the academic community in the field of applied mathematics, statistics and modeling, with the ICT system providers capable of developing advance software solutions, including aspects of design for manufacturability, and with the equipments suppliers supporting process evolution.

Projects could be small or large in terms of consortium size, cost or duration targeting fast return or longer term capability development. The large scale projects must target to involve the main actors in this field including large companies, IC manufacturers and Equipment and Materials suppliers, which will stimulate and organize the participation of supporting SMEs and Research Centers and Universities. These projects will be complemented by and open the way to the aggregation of smaller targeted and focused projects, if their suggested R&D content is significantly supportive to achieve the goals, with a large potential for SME contribution.

Indicative resources

600 PY for all SP8 target activities, representing 30% of the overall Work Programme.

Targeted start date: beginning 2009.

3 Requirements

The proposal should satisfy the following requirements.

Each proposal should address at least one Target Activity and one Sub-Programme and clearly identify which have been addressed.

All projects to be supported will be expected to identify, at proposal stage, their intended contribution to the achievement of the ENIAC SRA and AWP targets. Proposals should describe how projects would measure their contribution and how they would establish a baseline and thereafter monitor their progress compared with the baseline.

All projects are expected to have a strong industrial focus and present a realistic context for industrially relevant, short to medium term research and technology development, and to enable its validation. All projects should demonstrate their expected industrial, social or economic impact.

Clear expression of the technical approach to the research objectives will be essential.

All projects to be supported will be expected to share requirements and emerging results, during project execution, so as to achieve the coherent, synergistic progress sought by the ENIAC JU. All projects should demonstrate their possible synergy with other priorities, target initiatives or Sub-Programmes.

Project consortia must be balanced. Considering the explicit involvement of SMEs and favoring clustering of SMEs in innovation eco-systems is encouraged.

In view of the downstream research focus of the ENIAC JU and the targets described in this document, projects with duration longer than 3 years must provide adequate justification for their duration, relative to the application demonstrators and expected impact they describe.

4 Implementation of Call in 2008

4.1 Call 1: JU-ENIAC-1-2008

- Date of publication: 8th May 2008.
- Closure date: 3rd September 2008, at 17.00 h Brussels local time.
- Indicative ENIAC JU contribution to Call: 32 M€[5]
- Evaluation procedure: A one-stage submission procedure will be followed. The evaluation and selection procedure is described in the document: "ENIAC Joint Undertaking selection and evaluation procedures related to Calls for proposals". The evaluation criteria and sub-criteria are set out in section 5 of this Work Programme. The general eligibility criteria are listed in Annex.
- Indicative evaluation and contractual timetable: It is expected that the contract negotiations for the selected proposals will start as of November 2008
- Project agreements: Participants in all actions resulting from this call are required to conclude a project agreement.
- The grant which will be offered by the JU will be specified in the Grant Agreement applicable to ENIAC.

5 Evaluation Criteria for Proposals

Evaluation scores will be awarded for each of the five criteria, and not for the sub-criteria. Each criterion will be scored out of 10. No weightings will apply. The threshold for the individual criteria (1), (2), (3), (4) will be 6. There is no threshold for the individual criterion (5). The overall threshold, applying to the sum of the five individual scores, will be **35**.

The evaluation criteria against which proposals will be judged are:

1. Relevance and contributions to the content and objectives of the Call.
    - Relevance will be considered in relation to the Work Programme open in a given call.
2. R&D innovation and technical excellence.
    - Soundness of the concept and quality of the scientific and technological objectives.
    - Progress beyond the state-of-the-art.
3. S&T approach and work plan
    - Quality and effectiveness of the S&T methodology and associated work plan.
4. Market innovation and impact
    - Contribution to the expected impacts listed in the Work Programme under the relevant Sub-Programme and to the general ENIAC SRA and AWP targets.

[5] estimated as 55% of the amount of 58 M€ committed by ENIAC member States to the budget of this 2008 Call.

- Expected industrial, economic or societal impact
- Appropriateness of measures for the dissemination and exploitation of project results.
- Contribution to standards
- Management of intellectual property.

5. Quality of consortium and management.
   - Appropriateness of the management structure and procedures
   - Quality and relevant experience of the individual participants
   - Quality and balance of the consortium as a whole including complementarities and involvement of SMEs
   - Appropriateness of the level, allocation and justification of the resources to be committed (budget, staff, equipment)

6 How to submit a proposal

Proposals should be submitted in accordance with the terms set out in the call for proposals. In order to submit a proposal, applicants should consult the following documents:

- The text of the call for proposals, as announced in the Official Journal of the European Union and published on the webpage of the ENIAC Joint Undertaking
- This Work Programme
- ENIAC Eligibility criteria
- The Guide for Applicants

7 References

There are also a number of other useful texts which applicants could refer to:

AENEAS Articles of Association (http://www.eniac.eu)

Council Regulation 72/2008 (http://eur-lex.europa.eu)

ENIAC Multi-Annual Strategic Plan – version 1

Strategic Research Agenda of the European Technology Platform ENIAC (http://www.eniac.eu/web/downloads/SRA2007.pdf);

White book of Eureka cluster CATRENE: (http://www.catrene.org/web/calls/whitebook2.php)

8 Annex Eligibility Criteria for Proposals

8.1 Eligibility Criteria for Proposals

A proposal must satisfy all of the following eligibility criteria in order to be retained for evaluation:

- It is submitted using the ENIAC Proposal Service (EPS)
- It is received by the ENIAC JU before the deadline given in the call text.
- It involves at least 3 non-affiliated[6] legal entities established in at least 3 ENIAC member States (the list of ENIAC member States is published in the Call).
- It is complete and the following elements are present in the proposal as requested in the Guide for Applicants:
  - the administrative forms
  - the proposal description with all the mandatory sections
- It is submitted in English[7].
- The content of the proposal relates to the topic(s) described in the Annual Work Programme of the Call.

Only proposals that satisfy the above eligibility criteria are receivable and will be evaluated by the ENIAC Joint Undertaking.

If it becomes clear before, during or after the evaluation phase that one or more of the proposal eligibility criteria have not been fulfilled, the proposal will be declared ineligible by the ENIAC JU and will be withdrawn from any further examination. Where there is a doubt on the eligibility of a proposal, the ENIAC JU reserves the right to proceed with the evaluation, pending a final decision on eligibility. The fact that a proposal is evaluated in such circumstances does not constitute proof of its eligibility. The results of such an evaluation shall not be taken into consideration till a final decision on eligibility has been taken. In such a case the process of the proposal will be suspended until a final decision has been taken.

8.2 Eligibility Criteria for JU funding of individual participants

For all participants in proposals that have passed the eligibility criteria for proposals (section 2.1 above), the ENIAC Joint Undertaking will carry out the necessary verifications against the following eligibility criteria for ENIAC JU funding, on the basis of verifications carried out by the European Commission. The ENIAC JU eligibility criteria for funding are the following:

- The participant has its location in an EU Member State or in an Associated Country to the Seventh Framework Programme[8].

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[6] 'affiliated entity' means an affiliated entity as defined in Article 2 of the Regulation (EC) No 1906/2006.

[7] Except for the additional information and forms that may be requested by ENIAC member States for the verification of eligibility of national funding that can be in their respective national languages

- Grants may not be awarded to applicants who are, at the time of the grant award procedure, in one of the following situations:
  - they are bankrupt or in the state of being wound up, are having their affairs administered by the courts, have entered into an arrangement with creditors, have suspended business activities, are the subject of proceedings concerning those matters, or are in any analogous situation arising from a similar procedure provided for in national legislation or regulations;
  - they have been convicted of an offence concerning their professional conduct by a judgment which has the force of *res judicata*;
  - they have been guilty of grave professional misconduct proven by any means which the Joint Undertaking can justify;
  - they have not fulfilled obligations relating to the payment of social security contributions or the payment of taxes in accordance with the legal provisions of the country in which they are established or with those of the country of the Joint Undertaking or those of the country where the contract is to be performed;
  - they have been the subject of a judgment which has the force of *res judicata* for fraud, corruption, involvement in a criminal organization or any other illegal activity detrimental to the Communities' financial interests;
  - they are currently subject to an administrative penalty imposed by the Community institutions as referred to in the general Financial Regulation.
  - they are subject to a conflict of interest;
  - they are guilty of misrepresentation in supplying the information required by the Joint Undertaking as a condition of participation in the grant award procedure or fail to supply this information;

In addition, according to the Council Regulation, project participants established in ENIAC member States are eligible for funding from the ENIAC JU **after conclusion of a national grant agreement for such project with their corresponding national authority** following the award procedures of the ENIAC Joint Undertaking[9] and provided that such national authority has signed an 'administrative agreement' with the ENIAC JU[10]. The ENIAC JU will not conclude a grant agreement with a national participant from an ENIAC member State if a corresponding national grant agreement is foreseen but has not been concluded.

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[8] These are currently: Albania, Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Israel, Italy, Latvia, Liechtenstein, Lithuania, Luxembourg, FYR Macedonia, Malta, Montenegro, Netherlands, Norway, Poland, Portugal, Romania, Serbia, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey, United Kingdom. Please consult the most recent information on the list of Associated Countries to FP7 in *ftp://ftp.cordis.europa.eu/pub/fp7/docs/third_country_agreements_en.pdf*

[9] According to the ENIAC Joint Undertaking selection and evaluation procedures related to Calls for proposals, ENIAC member States may decide to establish grant agreements and fund organisations that are full partners in projects from other EU Member or Associated States of the Framework Programme. In this case, these organisations can be considered as national participants from the ENIAC member States awarding the grant agreements.

[10] According to the Council Regulation, the ENIAC JU and ENIAC member States will establish administrative arrangements in order to enable the implementation of projects and the granting of public funds

For the following applicants, the condition described in the preceding paragraph (previous conclusion of a national grant agreement) does not apply:

- legal entities established in Member States or Associated Countries to the Seventh Framework Programme that are not ENIAC member States[11]
- the Joint Research Center (JRC)
- international organisations having a seat in EU Member States or Associated Countries to the Seventh Framework Programme

[11] Unless stipulated otherwise in 'administrative agreement' that national authorities of these countries that are not ENIAC member States may have signed with the ENIAC JU. Currently there are no countries in this situation.